Development and characterizations of fine pitch flip-chip interconnection using silver sintering

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***Abstract* — Flip-chip interconnects made of silver are promising candidates to overcome the intrinsic limits of solder-based interconnects and match the demand for increased current densities of high-performance microprocessors. Dip-based interconnects have been demonstrated to be a promising approach to form electrical interconnects by sintering paste between copper pillars and pads. However, the quality of the process is limited by residual porosity and poor performances of the sintered joint formed between the pillar and the pad during sintering if a pressure > 50 MPa is not applied in order to decrease the final porosity. In this study, development has been focused on varying key dipping process parameters allowing a pressureless sintering process. Dip-transfer process was optimized on test vehicle and has shown electrical continuity over 700 interconnections with diameter down to 50 µm. We demonstrate high reliability of the process with microstructural observations, tomography X and thermal cycle up to 200 cycles without breakdown.**

Keywords — packaging, flip-chip, silver sintering, fine pitch, low temperature

I. INTRODUCTION

The constant growth of the electronic market and the increase in processor performance, thanks to advanced nodes, require the development of new packaging interconnect solutions (process and material) to preserve electronics device functionality. [1] Depending on the application, interconnects need to transmit signals at high bandwidths (e.g. for artificial intelligence) or high currents (e.g. for power devices). Furthermore, in SiP or 3D packaging, interconnections must be able to withstand multiple annealing during the integration process. This leads to a current interest for flip-chip interconnect, showing pitches below 200 µm. [2]

Some strategies have been developed to reduce interconnects' pitch in flip-chip assembly, such as micro-tubes [3] or hybrid bonding [4]. Currently, the most extensive strategy used to reduce the size and pitch of interconnects is the copper (Cu) pillar technology, capped on the tip by solder bump (micro-bump). [5-8] The bonding is formed by reflow, with temperature up to 250°C, in order to melt the solder alloy capping the Cu-pillars. This range of temperature can generate thermomechanical stress in the previous material interconnect used, for instance, in 3D stacking of components. In addition, the presence of solder joint in the interconnect leads to the formation of intermetallic compounds (IMCs) that are brittle, and to the formation of Kirkendall voids that reduce interconnects' reliability during operating time. [9-10]

Silver sintering process is currently a promising alternative to overcome intrinsic limits of solder bumps as die-attach technique in terms of thermal stability, while benefiting of better electrical and thermal performances. Compared to solder alloys, silver sintering allows to process at lower temperature and to stack components with temperature-resistant interconnects. Hence, recent developments of low-temperature pressureless sintering (LTPS) process have extended the application area of this process to mechanically sensible assemblies, as well as high-temperature power devices. [11-13]

Presently, the sintering process interconnect is mostly used to bond the back of chip onto substrate. In order to adapt this process to flip-chip interconnects such as nanofoam on top of Cu-pillars. [14-15] However, the elaboration of the nanofoam would increase cost, time and complexity of fabrication, whereas a significant bonding pressure (100 MPa) has to be applied to form interconnects. Also, electrically bond has not yet be demonstrated. Another strategy recently developed, is the photolithography process, associated to screen-printing, in order to form precise pattern made of sintering paste. [16-17] Drying of the deposited paste is necessary in order to strip off the resin from the substrate without damaging paste patterns. LTPS process needs highly reactive metallic content, such as nanoparticles. Whereas pre-drying step allows fixing deposited paste, huge loss of reactivity happens and makes it difficult to ensure LTPS process.

Dip-transfer of sinter paste between Cu pillars and pads is a promising alternative to form flip-chip assembly using soft conditions process in order to reduce pads' size below 100 µm and avoiding waste of sintering paste as in photolithography. Currently, dip based interconnect formation have been studied using copper paste for all-copper interconnects by sintering between 200 °C and 250 °C in a batch oven under formic atmosphere. [18] Whereas sintering without pressure is considered, the best performances are obtained with a bonding pressure up to 50 MPa. The consequence of this bonding pressure is thinner sintered joints (1-3 µm) that would hardly compensate the inhomogeneity of the pillar height. A work of Zurcher *et al.* showed a resistivity almost 5 times of the copper resistivity without using pressure bonding. [19] Besides, ageing study has not yet be carried out.

This work presents an advance dip-based silver sintering approach for 50 µm interconnect. We investigate the robustness of the dip transfer process with variation of critical parameter process, aiming for the thickest silver interconnect in order to compensate Cu pillars height inhomogeneity while processing in soft conditions. Then, we report satisfying repeatability of the process with a significant number of electrical continuity obtained over 700 interconnects, using as optimized dip-transfer process. Finally, thermal cycling study displayed interconnects reliability in soft conditions.

II. Materials & Methods

A. Ag commercial paste

A commercial silver paste was used as referenced throughout this study (CT2700R7M, KYOCERA, Tokyo, Japan), made of micro triangular platelets, showing nanometer thickness, as presented in Fig.1.

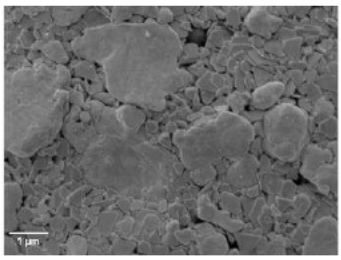

Fig. 1. SEM picture of KYOCERA paste before sintering.

B. Interconnect test vehicule

A specific test silicon chip was designed and fabricated for this study. It contains Cu pillars with a diameter of 50 µm, a pitch of 150 µm and a height of 75 µm. A 100 nm Au finish was deposited on the Cu pillars to prevent oxidation. (Fig.2.a,b) The 11.9 x 11.9 mm^2 sized chips were placed to a 22.1 x 14 mm^2 sized silicon substrates presenting Au-pads of 50 µm diameter. The global pattern test shows three Kelvin patterns (K) and five daisy chain patterns (DC) including 709 interconnects for 4-probes measurements, as presented Fig.2.c Aluminium-based routing has been passivated with 500 nm SiO_2 layer to ensure the precise measurement of interconnect in case of paste overflow. In addition, four lines of interconnect have been designed with Cu pillar with same diameter, height and pitch, and complete electric track along DCs pattern in order to detect the formation of bridges between interconnect after bonding pressure by an eventual spread of the silver paste. Further tests were performed with Cu pillars of smaller diameter and pitch of 35 µm and 105 µm respectively, with the same pattern test.

C. Ag interconnect formation

The process to form the silver interconnect is based on a dip-transfer method which is described Fig. 3. The chips containing the Cu pillars and the substrate were handled and aligned with a Datacon 2200 Evo (Besi, Netherlands). The commercial paste is applied in the device's cavity depth of 50 µm using its fixed gap applicator. The pillars were dipped into the silver paste film using the built-in dipping function of the datacon. Then, the pillars were withdrawn, aligned, and placed onto the substrate in order to transfer the silver paste collected. The flip-chip interconnect assembly was next transferred into an oven (UF55plus, Memmert) and heated for 1h under air at 250°C.

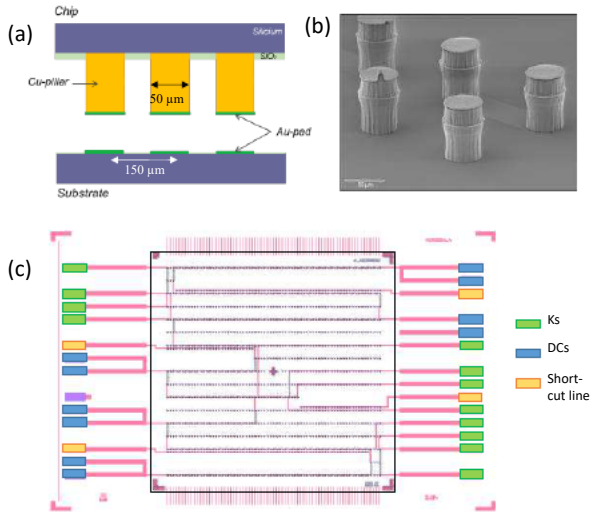

Fig. 2. (a) Scheme of test silicon chip containing Cu-pillar of 50 µm with 150 µm pitch ; (b) SEM images of Cu-pillar with Au-pad ; (c) scheme of the pattern test with 3 Ks, 5 DCs and 4 'short-cut lines'.

D. Interconnect characterization

After thermal treatment, tomography X analyses were carried out on the assembled parts in order to be assured that each interconnect was well formed (Nanotom S180, General Electric Research, US). Manual probes were used to carry out electric measurements onto the measurement pads of Kelvin and daisy chain pattern (PM8, SUSS Micro Tec, Germany). A Keithley 2400 multimeter was used to carry out 4-wire resistance.

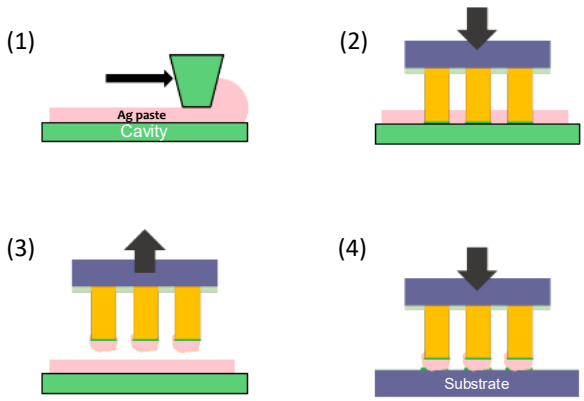

Fig. 3. Steps of the dip-transfer process in order to obtain silver sintered flip-chip assembly.

III. Results & Discussion

A. Optimization of dip-transfer process

Control over the collection of Ag paste on the pillar tips during dip-transfer is necessary to form silver interconnects with high yield, enough thickness to compensate height Cu-pillar mismatch (± 2 µm) and to avoid the paste spreading between interconnects.

The main parameters of the dip-transfer process were evaluated, such as the dipping time in the Ag-paste film, withdrawal velocity from the paste and bonding force, using the interconnect test vehicles described above. Other parameters were kept constant. Three chips were tested for each parameter. We found that the velocity withdrawal do not affect the morphology and thickness of the paste collected on the Cu-pillar tips (from 0.2 to 4 mm/s). This phenomenon was already observed in [19]. The increase of the bonding force do not favor the homogeneous formation of interconnect (1N, 3N and 5 N), hence, obtaining electric continuity overall the daisy chain is difficult (respectively 100 %, 50% and 0% viable). The highest bonding force used during the report of the chip favors a drag force between the tool of the datacon's head and the back of the chip that stays stuck. In hindsight, reducing the approach velocity of the datacon's head (50ms) at the bonding step, leading to a 'stamp effect', has shown increase in the interconnect formation yield.

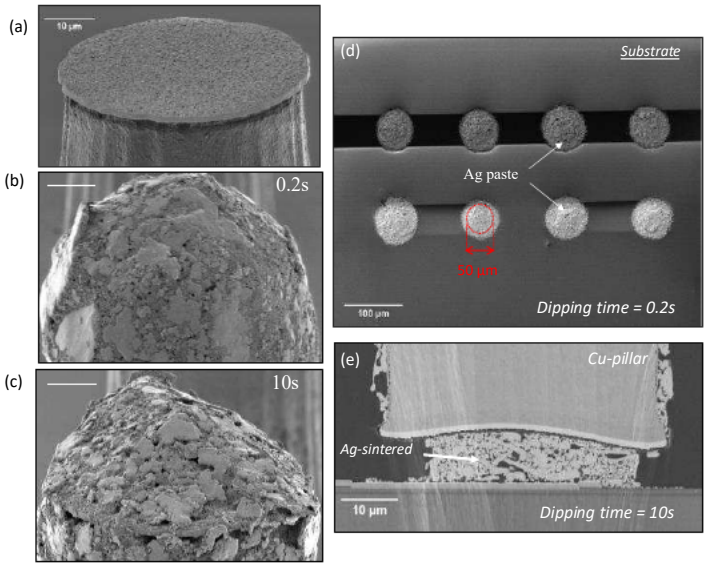

Fig. 4. (a)(b)(c) SEM observations of Cu-pillar tip before dipping, after 0.2 and 10s dipping ; (d) SEM observation of the 'wetting diameter' of the silver paste using 0.2s dipping time ; (e) Cross-section of silver sintered interconnect using 10s dipping time, showing 8-10 µm of thickness.

The dipping time has been shown to be the parameter with the most influence over the dipping process to obtain a precise coating of the Cu-pillar tips. (Fig.4.a, b, c) Lower dipping time (0.2s) favors inhomogeneous coating of the pillars. While the coating tends to be thicker and rounder, we estimated the 'wetting area' of the paste deposits after assembly, as they are squeezed between Cu-pillar and Au-pads on the substrate. The 'wetting diameters' were greater than the pillars' diameter and rather inhomogeneous (65 ± 5 µm vs. 50 µm), but no bridges were observed. (Fig.4.d.) Substantial increase of the dipping time (10s) reduces the coating to a reasonable amount of paste at the top of the Cu-pillars. Cross-sections show most interconnect with diameters below 35 µm, reducing paste spreading risks, with a satisfying thickness of 8-10 µm. (Fig.4.e) Finally, the dip-transfer process as optimized was proved robust with precise coating on the Cu-pillar tips in a single dip.

B. Electrical performances of the silver sintered interconnects

Silver interconnects were formed using the optimized parameters of the dip-transfer process. The final silver sintered bond were about 8-10 µm, with a diameter from 25 µm to 35 µm, sandwiched between Cu-pillar tips and the Au-pads of the substrate. No signal were obtained overall the batch of 4 'short-cut lines' on each sample, meaning that no bridges were ever formed due to paste spreading after assembly.

The overall electrical continuity of a batch of 8 samples was satisfying, with 5 out of 5 DCs (709 interconnects) were functional. Tomography X characterizations were carried out upon the assemblies showing defective DCs but also upon perfectly functional DCs. Electric continuity rely on each interconnect of the pattern : one faulty interconnect is enough to discriminate hundreds of them. We observed that each time a DC was defective, a Cu-pillar was missing. (Fig. 5.) The loss of Cu-pillar could be explain either by defect of fabrication process (missing aperture in the masks), or relative trauma when wafer were handled before experiments. This is not uncommon in industrial process scale to get a certain amount of partially damaged components. In our case, it would be easily spotted through optic microscopy observations.

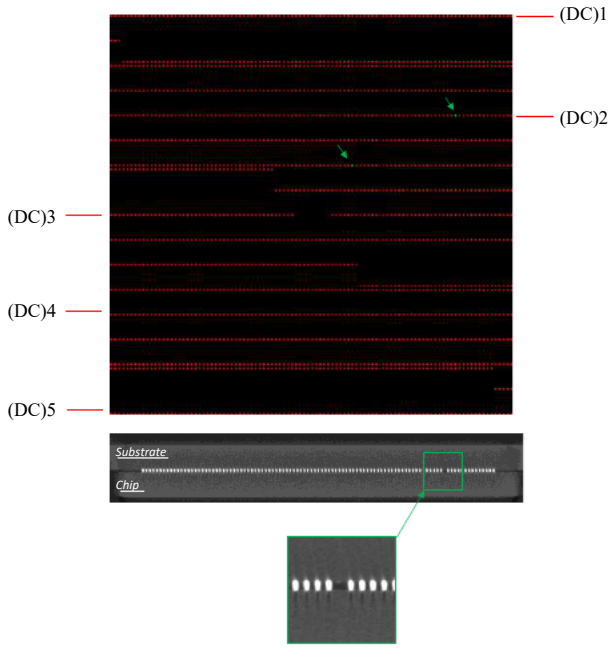

Fig. 5. Reconstruction after tomography X analyses of functional DCs (green) and dysfunctional DCs (red), showing two missing pillars correlating with only 3 functional DCs.

The average value measured for the 24 Ks patterns was 33.14 mOhms, with best value at 6.5 mOhms. The resistivity of one Cu-pillar obtained by electrolytic growth was estimated at 2.95 µOhm.cm. Hence, it is possible to estimate the global resistivity of the silver sintered layer and the two imperfect interfaces with Au-pads of the substrate and the Cu-pillar. The value of the resistivity estimated is around 56.7 µOhms.cm at best, i.e. 35 times the resistivity value of the Ag bulk.

Compared to the literature on this research topic for pressureless sintered interconnect, it is 100 times better.

C. Thermal cycling of the silver interconnects

Thermal cycling from -50°C to 150°C was carried out upon a batch of four samples presenting each 5 DCs. Over 200 cycles were achieved, leading to the failure of only one DC of one sample. After each 24 cycles, electric measurement of each DC showed slight decrease of the overall resistance value. (Fig.6.) This is one of the great advantages of sintered interconnects which benefit from the first heating to tend to a better densification throughout atomic diffusion between highly reactive particles and interdiffusion with metal finishes.

IV. Conclusion

In this study, by varying key dipping process parameters, a reliable dip-transfer method has been developed, leading to the formation of relatively thick silver interconnect (8-10 µm) allowing to compensate eventual mismatch height between Cu-pillars. Dip-transfer process as optimized has shown electrical continuity over 700 interconnections with diameter down to 50 µm, 150 µm pitch, suitable to endure over 200 cycles from -50°C up to 150°C with slight increase of the electrical performances during the thermal cycling. We have demonstrated with tomography X analyses that dysfunctional DCs comes from previously missing Cu pillar.

V. Outlook

First tests have been done on interconnects of 35 µm with great success, showing similar issue with previously missing Cu pillars. Further mechanical characterizations before and after thermal cycling in order to estimate the reliability of the silver interconnect as obtained. In order to soften the sintering conditions with temperature at 185 °C, and to favor well-densified bond, a nanopaste made of silver nanocubes will be elaborated with, this time, the rheological properties needed for dip-transfer process. [20]

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